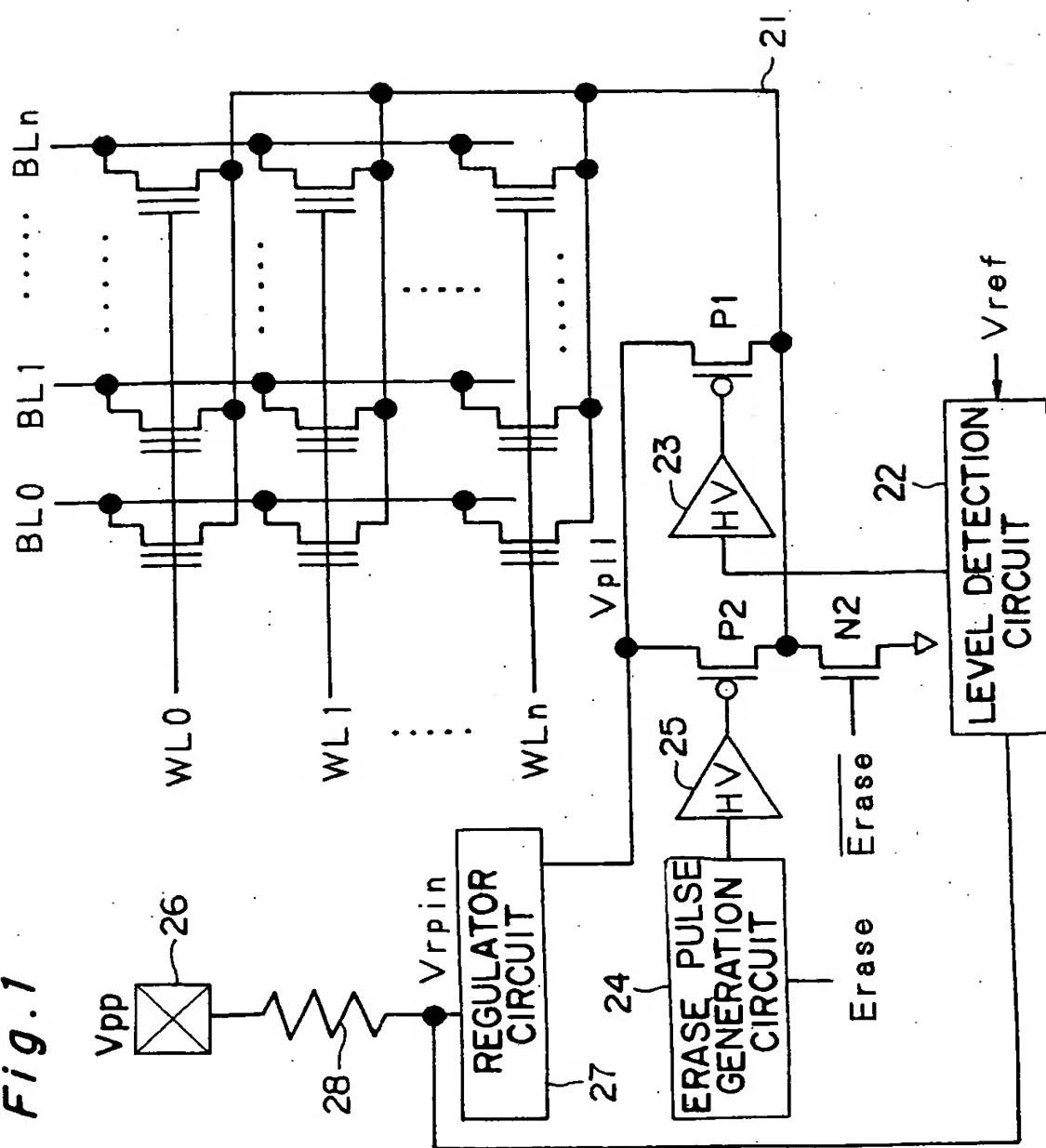


Fig. 1



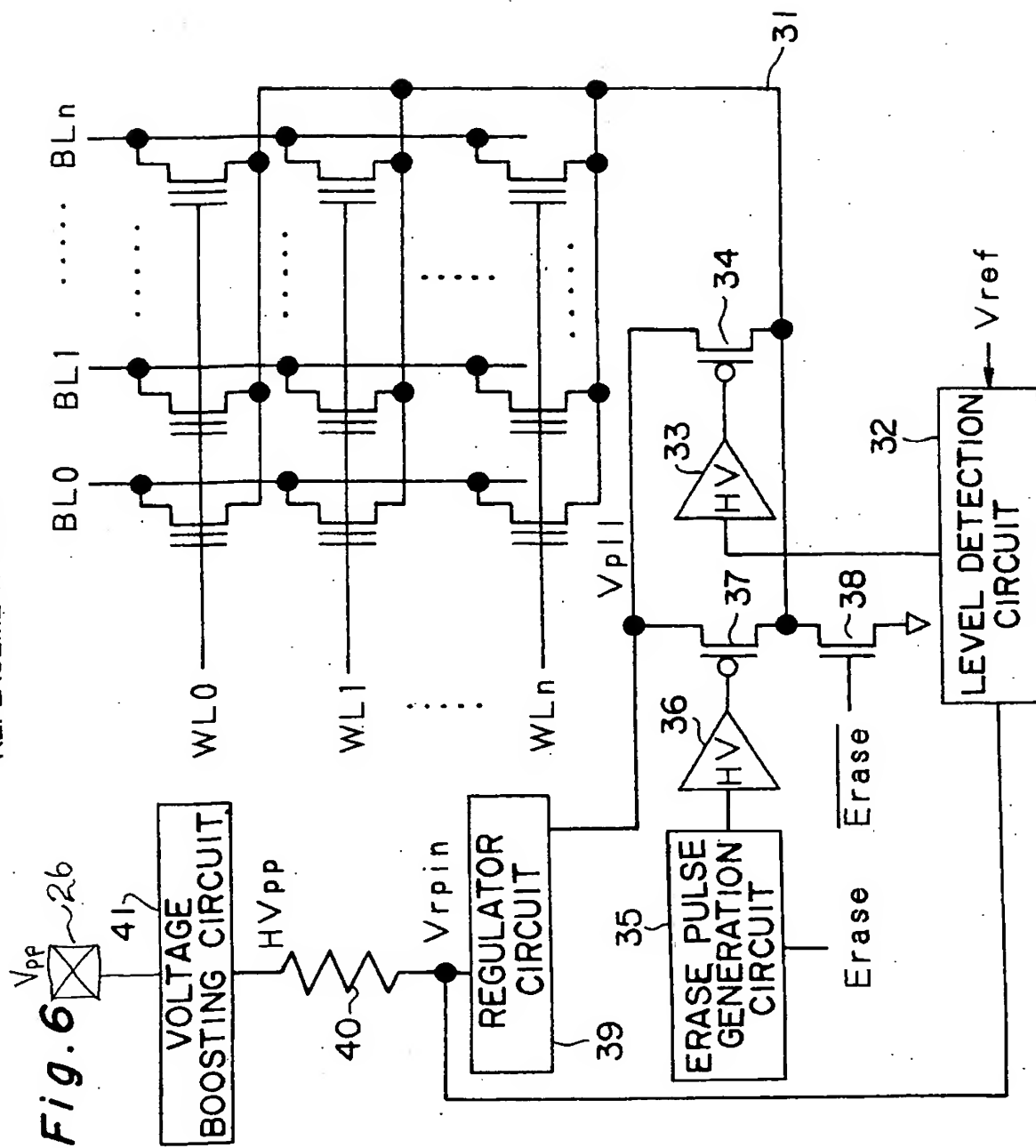
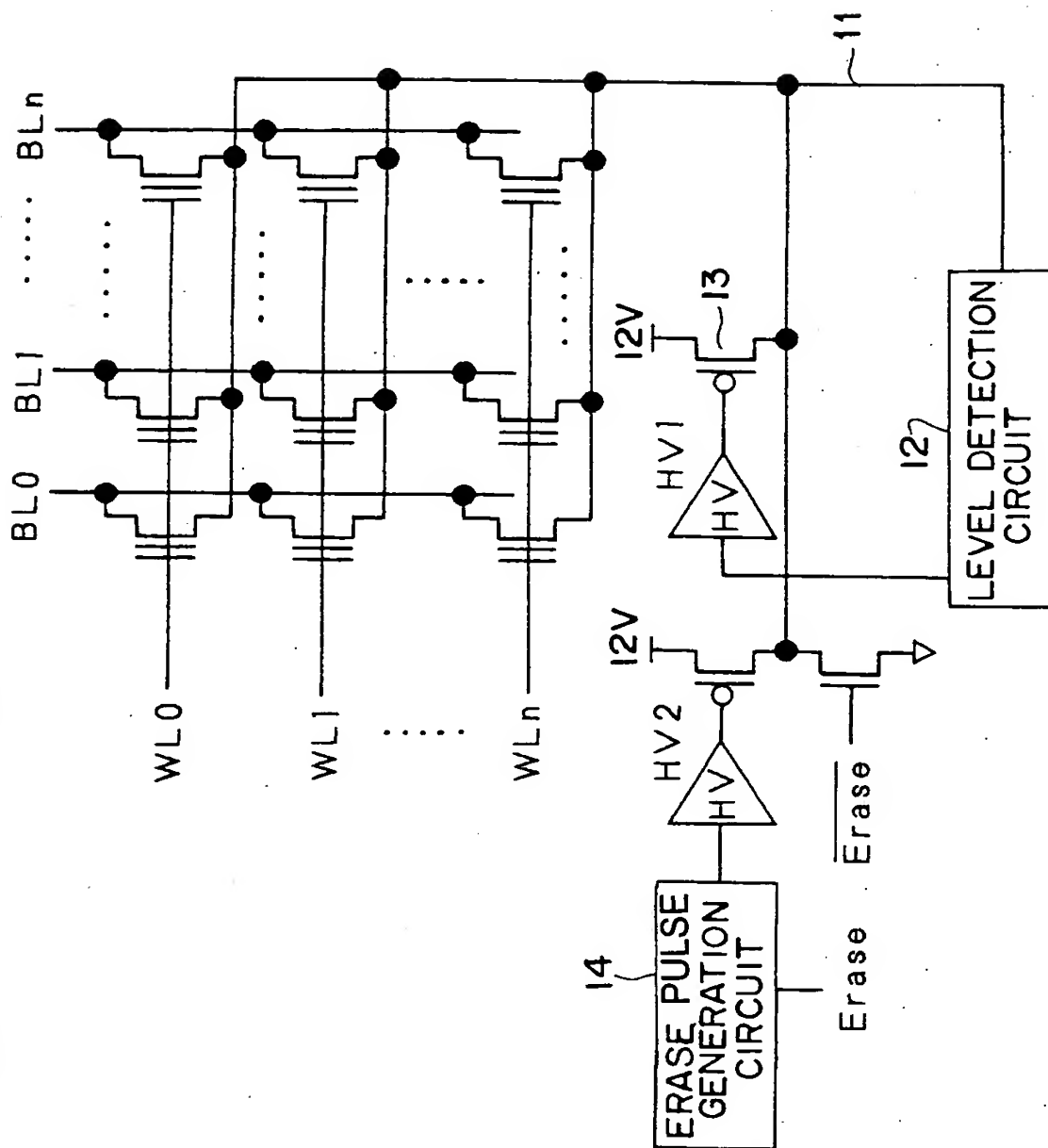




Fig. 15 PRIOR ART



The schematic diagram illustrates a memory array structure. The array consists of multiple word lines (WL0, WL1, ..., WLn) and bit lines (BL0, BL1, ..., BLn). Each word line is connected to a series of access transistors, which are in turn connected to a series of storage capacitors. The storage capacitors are connected to the bit lines. The bit lines are connected to sense amplifiers (16) and a level detection circuit (15). The sense amplifiers (16) are connected to the bit lines and provide a 5V output. The level detection circuit (15) is connected to the bit lines and provides an Erase signal to the Erase Pulse Generation Circuit. The Erase Pulse Generation Circuit is connected to the Erase signal and provides a 5V output to the sense amplifiers (16). The level detection circuit (15) also provides a 5V output to the sense amplifiers (16).